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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/978,420	10/15/2001	Kuo-Yu Chou	67,200-409	5300

7590 02/09/2005

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ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/09/2005

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/978,420
Filing Date: October 15, 2001
Appellant(s): CHOU ET AL.

Randy W. Tung
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1/5/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

This appeal involves claims 1-3, 6 and 13.

Claims 4, 5 and 7-12 been canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US 2002/0155672 A1	Wang et al.	10-2002
US 6,392,300	Koike	5-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3, 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 2002/0155672 A1) in view of Koike (U.S. Patent No. 6,392,300 B1).

Wang et al. teach in figures 1-4 and in paragraphs 1-23 a method for fabricating a microelectronic fabrication.

With regard to claim 1, Wang et al. teach a method comprising:

providing a substrate 100 (figure 1);

forming over the substrate a series of patterned conductor layers 102 separated by a series of dielectric layers (figure 1, paragraphs 6-8 and 17); and

forming over the substrate in electrical communication with the series of patterned conductor layers 102 separated by the series of dielectric layers at least one fuse layer 112 (figure 2 shows the fuse layer 112 formed and figures 3 and 4 show the fuse layer after being patterned into fuses 112b and bondpad 112b), wherein the at least one fuse layer 112 is formed at a level no lower than a highest of the series of patterned conductor layers 102 and wherein the at least one fuse layer 112 and the highest of the series of patterned conductor layers 102 are formed of different conductor materials.

Wang et al. teach in paragraphs 6-8 the use of fuses to connect normal memory cell arrays and redundant memory cell arrays where the fuse is formed on the uppermost layer of the semiconductor device, the same level as the bond pad. Though the figures show a single patterned conductive layer 102 with fuses over it, it is inherently understood that the semiconductor substrate would include many patterned conductive layers separated by a series of dielectric layer for each memory array and that the fuses would be connected to some of the patterned conductive layers to allow for the fuses to substitute defective memory cells.

Wang et al. do not teach forming the fuse layer simultaneously with an alignment mark.

Koike teach a method of forming a microelectronic fabrication in figures 1-9 and on columns 1-3 for example. Koike teach providing a substrate 11 (figure 1), forming over the substrate a series of patterned conductor layers 18, 21, 24 (figures 2-4) separated by a series of dielectric layers 19, 22 (figures 3 and 4), and forming an

alignment mark 27A simultaneously a fuse (not shown) or bond pad 27B (figure 5, column 2 lines 8-11).

Wang et al. and Koike are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an alignment mark simultaneously with the fuse layer in an upper metal layer. The motivation for doing so is to provide an alignment mark for positioning a laser to allow for blowing of the fuse. Therefore, it would have been obvious to combine Wang et al. with Koike to obtain the invention of claim 1.

With regard to claim 2, Wang et al. teach the microelectronic fabrication selected from integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

With regard to claim 3, Wang et al. teach the at least one fuse layer is formed simultaneously with a bond pad layer within the microelectronic fabrication in figures 3 and 4 as the same layer 112 is etched to form both the fuse and the bond pad.

With regard to claim 6, the at least one fuse layer is formed of an aluminum containing conductor material and the highest of the series of patterned conductor layers is formed of a copper containing conductor material.

With regard to claim 13, Wang et al. teach a method comprising:

providing a substrate 100 (figure 1);

forming over the substrate a series of patterned conductor layers 102 separated by a series of dielectric layers (figure 1, paragraphs 6-8 and 17); and

forming over the substrate in electrical communication with the series of patterned conductor layers 102 separated by the series of dielectric layers at least one fuse layer 112 (figure 2 shows the fuse layer 112 formed and figures 3 and 4 show the fuse layer after being patterned into fuses 112b and bondpad 112b), wherein the at least one fuse layer 112 is formed at a level no lower than a highest of the series of patterned conductor layers 102 and wherein the at least one fuse layer is formed simultaneously with a bond pad.

Wang et al. teach in paragraphs 6-8 the use of fuses to connect normal memory cell arrays and redundant memory cell arrays where the fuse is formed on the uppermost layer of the semiconductor device, the same level as the bond pad. Though the figures show a single patterned conductive layer 102 with fuses over it, it is inherently understood that the semiconductor substrate would include many patterned conductive layers separated by a series of dielectric layer for each memory array and that the fuses would be connected to some of the patterned conductive layers to allow for the fuses to substitute defective memory cells.

Wang et al. teach the at least one fuse layer is formed simultaneously with a bond pad layer within the microelectronic fabrication in figures 3 and 4 as the same layer 112 is etched to form both the fuse and the bond pad.

Wang et al. do not teach forming the fuse layer simultaneously with an alignment mark.

Koike teach a method of forming a microelectronic fabrication in figures 1-9 and on columns 1-3 for example. Koike teach providing a substrate 11 (figure 1), forming over the substrate a series of patterned conductor layers 18, 21, 24 (figures 2-4) separated by a series of dielectric layers 19, 22 (figures 3 and 4), and forming an alignment mark 27A simultaneously a fuse (not shown) or bond pad 27B (figure 5, column 2 lines 8-11).

Wang et al. and Koike are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form an alignment mark simultaneously with the fuse layer in an upper metal layer. The motivation for doing so is to provide an alignment mark for positioning a laser to allow for blowing of the fuse. Therefore, it would have been obvious to combine Wang et al. with Koike to obtain the invention of claim 13.

(10) Response to Argument

Appellant first puts forth arguments in response to a first instance. Appellant argues that Koike teaches that only either a bond pad or a fuse layer is formed simultaneously with an alignment mark, but not both a bond pad and a fuse layer is

formed simultaneously with the alignment mark. Appellant furthers this argument in stating that Koike implicitly teaches that an alignment mark may not be formed when a fuse layer and a bond pad are present and thus Koike teaches away from forming all three (thus teaching away from the combination). First the examiner does not rely on Koike to teach forming all three structures (the bond pad, alignment mark, and the fuse layer) simultaneously but merely relies on Koike to teach forming the fuse layer simultaneously with an alignment mark. The issue at hand is whether Koike, in using the term "or" (column 6 lines 24-27), has explicitly taught that the fuse and the bond pad can not both be formed simultaneously with an alignment mark. The Appellant has taken the position that in using the term "or" Koike is explicitly teaching that all three structures can not be formed at the same time. This position is incorrect. Koike merely states that one or the other of the bond pad and fuse layer is formed simultaneously with the alignment mark, not that ONLY one of the bond pad and fuse layer can possibly be formed simultaneously with the alignment mark. Koike's teaching of forming the bond pad or the fuse layer does not preclude both the bond pad and fuse layer being formed simultaneously. In fact, taking into account the rejection as a whole, we see that Wang et al. explicitly teaches that the fuse layer can and is formed simultaneously with the bond pad. Koike does not explicitly or implicitly teach away from the combination. Koike merely lacks a teaching of forming both the bond pad and the fuse layer simultaneously with an alignment mark. The fact that a reference lacks teaching a specific limitaiton claimed does not mean that the reference teaches away from a combination with a second reference that does teach the missing limitation.

Appellant further puts forth arguments in resonse to a second instance. Appellant argues that Wang and Koike may not properly combined incident to the Examiner's first rationale directed toward their mere existence in the same field of endeavor, since the same provides an insufficient basis to establish prima facie obviousness. This is not persuasive as the Examiner has not porported that the sole basis for combining the references is the mere fact that they are from the same field of endeavor. The Examiner has provided motivation for why one of ordinary skill in the art would combine the references. As stated on the sentence spanning pages 3 and 4 of the Final Office Action, "the motivation for doing so is to provide an alignment mark for positioning a laser to allow for blowing of the fuse." The statement that the references are from the same field of endeavor is merely stating that they may be combined. This statement is merely one portion of the basis for establishing prima facie obviousness.

Appellant further puts forth arguments in resonse to a third instance. Appellant further argues that the rationalization for suggestion or motivation for modification or combining of Wang with Koike, while applicable to a specific situation taught within Koike, is not necessarily applicable to Wang.

Appellant also aruges that Wang might be reasonalby interpreted as apparently explicit as to absence of other exposable structures formed within Wang's microelectonic fabrication since they teach just a fuse layer and bond pad are exposed. This has no bearing on the combination of the references. The fact that Wang

themselves did not consider other exposable structures (for instance, the alignment mark) in the details of their disclosure does not preclude other references in the art teaching the desiribility of including other exposable structures like the alignment mark of Koike. The fact that Wang did not teach other structures is not the same as an explicit teaching that other structures may not exist.

Appellant further argues that although the alignment mark is formed simultaneously with the fuse layer is Koike this would not necessarily appeal to be a requirement of Koike's invention in that an alignment mark formed at an alternate level would appeal to function for alignment when severing a fuse. This is not relevant as Koike does not teach an alignment mark on an alternate level, Koike teach the alignment mark formed on the same level and simultaneously with the fuse. Whether an alignment mark could be formed elsewhere in the fabrication is irrelevant as the rejection relies upon the specific alignment mark taught by Koike, which is formed simultaneously with the fuse layer as claimed.

Appellant further argues that Wang may use one of their fuse layers as an alignment mark. This argument is merely speculation by the Appellant. That one might be able to use the fuse layers of Wang for a purpose (alignment) not disclosed or suggested by Wang is mere speculation that is not based upon any teaching in the reference. Further, if one of Wang's fuse layers is used as an alignment mark, as suggested by Appellant, Wang would then disclose all the limitations of the instant claims and would anticipate the claims under 35 U.S.C. 102.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

N. Drew Richards

Conferees:

Tom Thomas

Olik Chaudhuri

TOM THOMAS
SUPERVISORY PATENT EXAMINER